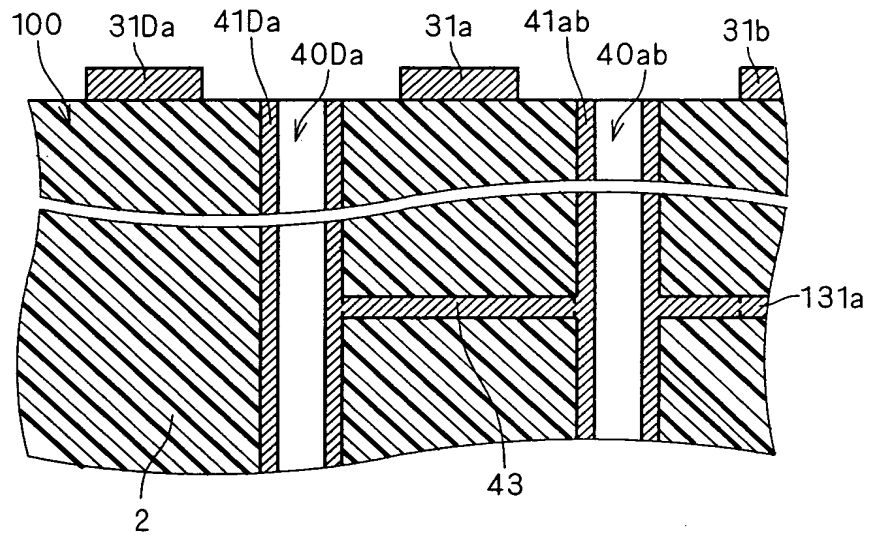
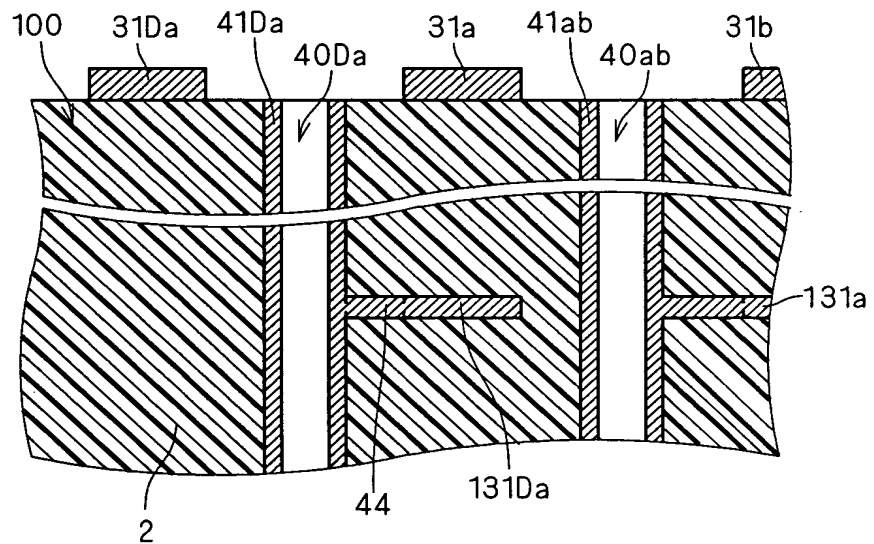




F I G . 5



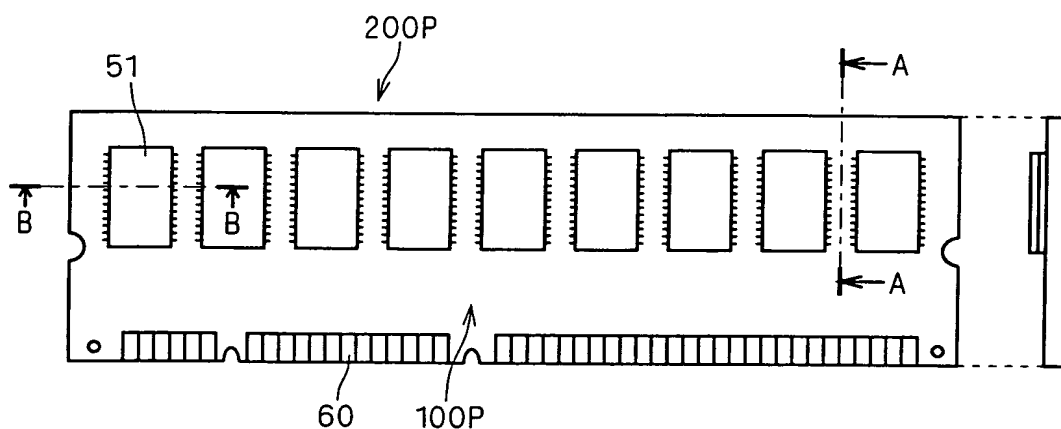
F I G . 6





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F I G . 15 PRIOR ART



F I G . 16 PRIOR ART

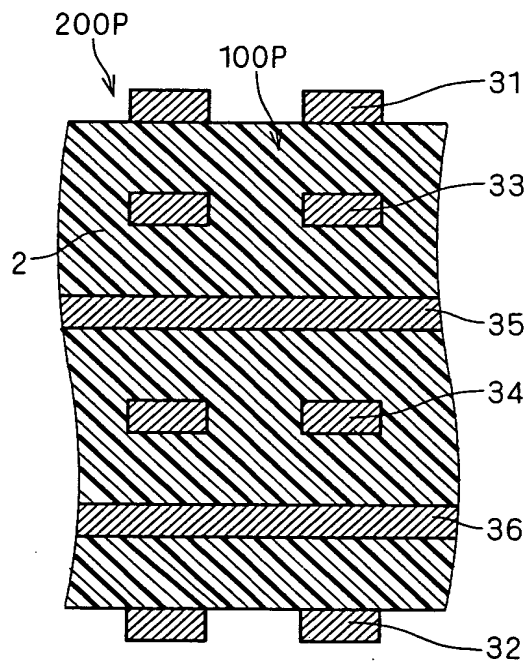
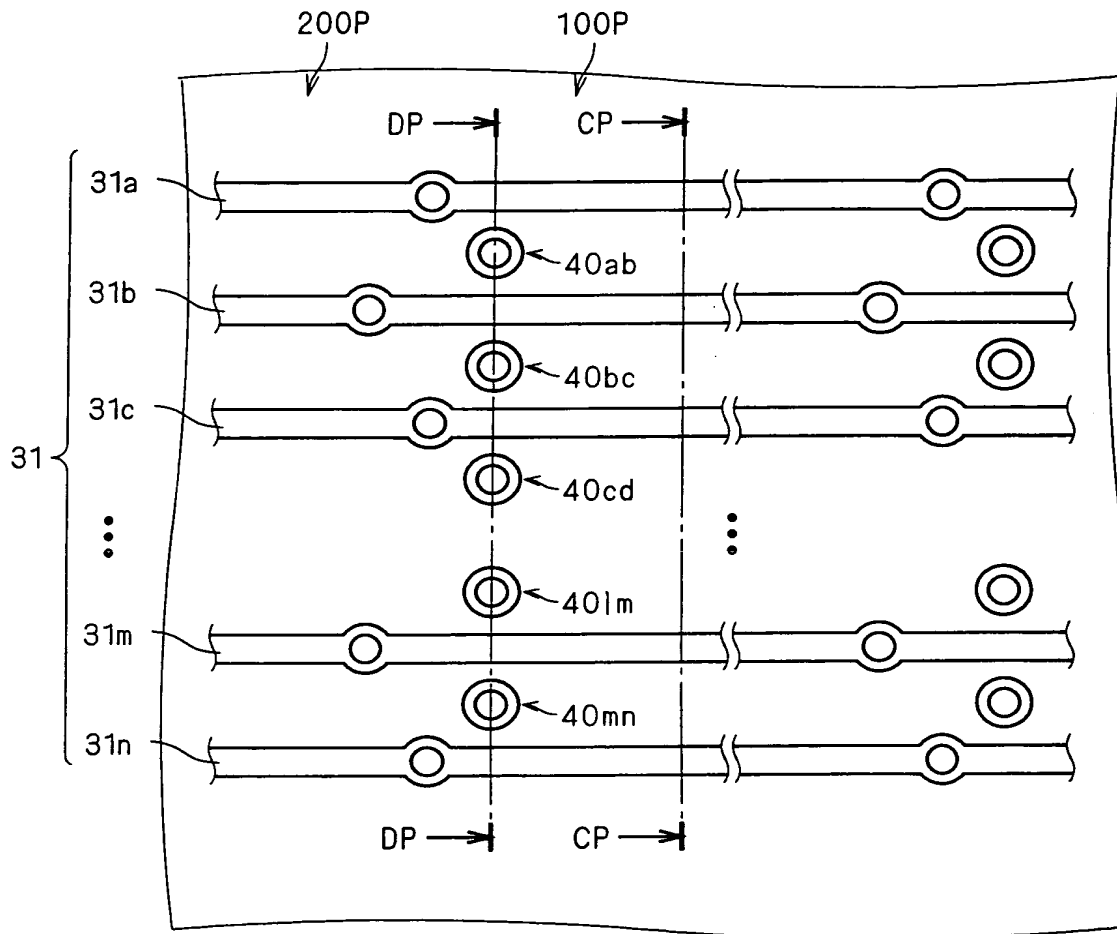




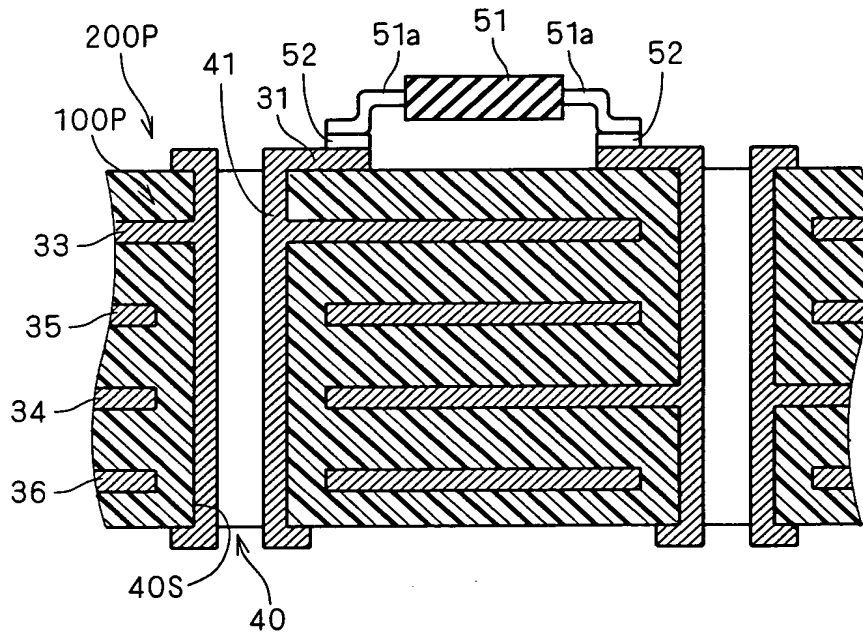
FIG. 17 PRIOR ART



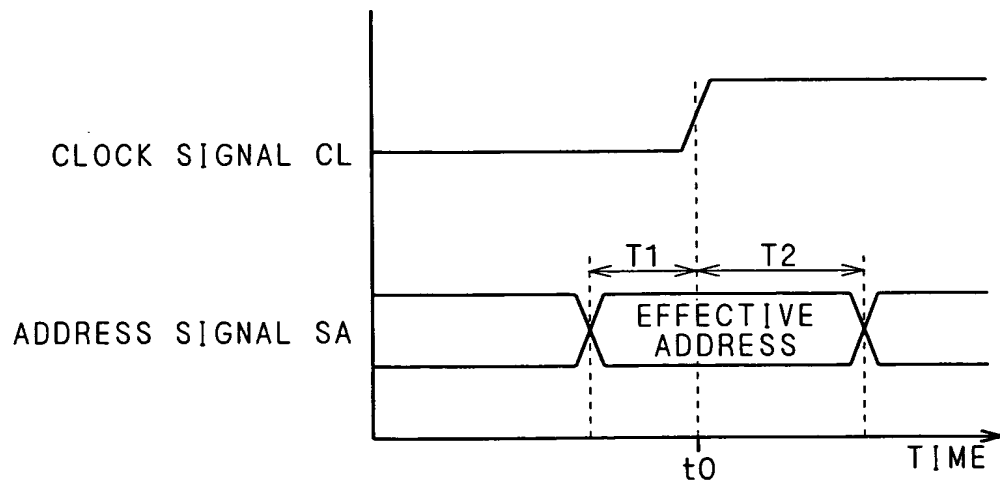


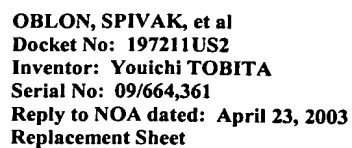
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F I G . 18 PRIOR ART



F I G . 19 PRIOR ART





A schematic diagram showing a series connection of capacitors. The circuit consists of a horizontal line with several components connected in series. From left to right, there is a shaded rectangular block labeled 31a, followed by a capacitor labeled CSW, then another shaded rectangular block labeled 31b, followed by another capacitor labeled CSW. This sequence is followed by an ellipsis (...) indicating more components, then another capacitor labeled CSW, and finally a shaded rectangular block labeled 31n. A large curly bracket underneath the entire series of components is labeled 31.

The diagram shows three signals over time: CLOCK SIGNAL CL, ADDRESS SIGNAL SA_a ~ SA_n, and ADDRESS SIGNAL SA_b ~ SA_m. The clock signal CL transitions from low to high at time t_0 . The address signals SA_a ~ SA_n and SA_b ~ SA_m are shown as pulses that are effective during a specific time window. The time interval from the rising edge of the clock to the start of the effective address is Δt . The time interval from the end of the effective address to the rising edge of the clock is T_3 . The time interval from the start of the effective address to the end of the effective address is T_1 . The time interval from the end of the effective address to the rising edge of the clock is T_2 . The time interval from the rising edge of the clock to the end of the effective address is Δt .